REMARKS

Claims 1-95 are pending in the present application. The Examiner has rejected claims 1-95.

I. *REJECTION OF CLAIMS 1-18, 20-38, 40-59 AND 61-94 UNDER 35 U.S.C. § 103(a)*

Claims 1-18, 20-38, 40-59 and 61-94 stand rejected under 35 U.S.C. § 103(a) as being obvious over U.S. Patent No. 6,194,962 B1 ("Chen") in view of U.S. Patent No. 4,901,030 ("Webster"). Applicants respectfully traverse the rejection.

A. Claims 1-18, 20 and 21

To maintain an obvious rejection, each and every element must be taught by Chen in view of Webster as alleged by the Examiner. Applicants respectfully disagree that, as alleged by the Examiner, Chen in view of Webster teaches each and every element. For example, Chen in view of Webster as alleged by the Examiner does not teach each and every element as recited in claim 1. Claim 1 recites, for example, "a plurality of differential pairs coupled together though a common differential output".

First, the Examiner has never expressly acknowledged that there is a difference between "differential pairs coupled together through a common differential output" and "a plurality of differential pairs coupled together through a common differential output" as set forth in claim 1. The Examiner's evidence is limited to transistors MN1 and MN2 in Chen which allegedly form a differential pair. However, the Examiner never explains how Chen teaches "a plurality of differential pairs coupled together through a common differential output". Applicants respectfully challenge the Examiner to provide document support for a plurality of differential pairs coupled together through a common differential output (which presumably is a lot harder than merely showing a single differential pair coupled together through a common differential output).

Second, the Examiner admits that Chen does not teach or suggest *a plurality* of differential pairs coupled together through *a common differential* output. Instead, the Examiner alleges that Webster makes up for the teaching deficiencies of Chen. Presumably, Webster teaches a plurality of differential pairs coupled together through a common differential output. Instead of merely pointing to the reference numbers in the figure in Webster or to the one line in the specification of Webster that clearly shows a plurality of differential pairs coupled together through a common differential output, the Examiner provides an explanation completely devoid of pinpointing "a plurality of differential pairs coupled together through a common differential output" and cites an enormous amount of text – no of which discusses "a plurality of differential pairs coupled together through a common differential output". Applicants can only attempt to try to decipher the clues left by the Examiner as to where Applicants might possibly find "a plurality of differential pairs coupled together through a common differential output". Thus, Applicants respectfully analyze the text cited by the Examiner, namely, Webster at col. 1, line 41 to col. 2, line 42; col. 6, line 62 to col. 7, line 66; and col. 12, lines 15-52 in the following discussion.

Webster at col. 1, line 41 to col. 2, line 42 is, of course, nothing less than the entire SUMMARY OF THE INVENTION section. Applicants respectfully plead with the Examiner, in the future, if he know exactly where the relevant material in a reference is to kindly direct Applicants attention to the relevant line. Applicants are at a loss as to why the Examiner is unable to concisely cite the relevant text. The SUMMARY OF THE INVENTION section discusses no less than the entire architecture of an operational amplifier. Surely, the entire architecture of an operational amplifier is not relevant to directing Applicants text teaching "a plurality of differential pairs coupled together through a common differential output".

The SUMMARY section is broken down to the three main parts of an operational amplifier: an input stage 601, a gain stage 603, and an output stage 605 as illustrated as dashed blocks in FIG. 1 of Webster. Applicants respectfully draw the attention of the Examiner to FIG. 1 to which the SUMMARY section effectively describes. FIG. 1 of Webster shows the input stage 601, the gain stage 603, the output stage 605 and the bias circuit 607. It is clear that FIG. 1 only shows a single differential pair comprising transistors Q101, Q102. FIG. 1 does not show "a plurality of differential pairs". Furthermore, the output (i.e., the collector) of transistor Q101 is connected to the emitter of transistor Q2 and the output (i.e., the collector) of transistor Q102 is connected to the emitter of transistor Q1. Thus, not only does Webster not teach "a plurality of differential pairs", but Webster also does not teach "a plurality of differential pairs *coupled together through a common differential output*" (emphasis added).

Webster at col. 6, line 62 to col. 7, line 66 relates to FIGS. 1 and 4 of Webster. Applicants have already established that FIG. 1 does not teach "a plurality of differential pairs coupled together through a common differential output". Applicants draw the attention to FIG. 4 of Webster. FIG. 4 shows a schematic of the input stage 601 and part of the bias circuit 607 and part of the gain stage 603. As with FIG. 1, FIG. 4 only shows a single differential pair comprising the same transistors described above, namely, transistors Q101, Q102. Thus, for the

reasons above, not only does FIG. 4 not show "a plurality of differential pairs", FIG. 4 does not show "a plurality of differential pairs *coupled together through a common differential output*" (emphasis added).

Webster at col. 12, lines 15-52 relates to a Darlington pair of transistors. In particular, the Darlington pair of transistors QD, Q9 is illustrated in FIGS. 11 and 12. Applicants respectfully remind the Examiner that a Darlington pair is NOT a differential pair of transistors. Applicants respectfully draw the attention to transistors QD, Q9 in FIG. 11 which clear show that configuration is NOT a differential pair configuration. Applicants respectfully challenge the Examiner to point out the differential inputs and outputs to the Darlington pair of transistors QD, Q9. FIG. 12 merely shows another embodiment of transistor QD. Transistor QD, in FIG. 12, comprises current mirror transistors Q104A, Q104B, transistor Q8, resistor R4 and transistor Q105. Applicants respectfully submit that FIGS. 11 and 12 of Webster do not show any differential pairs and thus do not show "a plurality of differential pairs". Furthermore, FIGS. 11 and 12 of Webster do not show "a plurality of differential pairs *coupled together through a common differential output*" (emphasis added).

Having analyzed all the text in Webster cited by the Examiner in support of the obviousness rejection, it is clear that Webster at col. 1, line 41 to col. 2, line 42; col. 6, line 62 to col. 7, line 66; and col. 12, lines 15-52 and any and all the figures associated with the cited text do not teach "a plurality of differential pairs" and, in particular, the cited text and accompanying figures of Webster do not teach "a plurality of differential pairs *coupled together through a common differential output*" (emphasis added).

Since Webster does not make up for the teaching deficiencies of Chen, the combination of Chen in view of Webster does not teach each and every element as set forth in claim 1. Accordingly, Applicants have successfully traversed the obviousness rejection with respect to claim 1 and its dependent claims (i.e., claims 2-18, 20 and 21).

It is respectfully requested that the rejection under 35 U.S.C. § 103(a) be withdrawn with respect to claims 1-18, 20 and 21.

B. Claims 22-38, 40 and 41

To maintain an obvious rejection, each and every element must be taught by Chen in view of Webster as alleged by the Examiner. Applicants respectfully disagree that, as alleged by the Examiner, Chen in view of Webster teaches each and every element. For example, Chen in view of Webster as alleged by the Examiner does not teach each and every element as recited in claim 22.

The Examiner alleges that Chen teaches each and every element as set forth in claim 22 except "the first nodes of the first transistors being coupled together and the first nodes of the second transistors being coupled together to form a differential output". Applicants disagree and note that Chen does not teach at least "a plurality of amplifying stages each having first and second transistors, the first and second transistors each having first, second and third nodes, the first nodes of the first transistors being coupled together and the first nodes of the second transistors being coupled together to form a differential output" as set forth in claim 22. Webster also does not teach at least these elements.

To support the obviousness rejection, the Examiner alleges that Webster makes up for the teaching deficiencies of Chen by teaching "the first nodes of the first transistors being coupled together and the first nodes of the second transistors being coupled together to form a differential output". To support this assertion, the Examiner cites the same text as before with respect to the rejection of claim 1, namely, Webster at col. 1, line 41 to col. 2, line 42; col. 6, line 62 to col. 7, line 66; and col. 12, lines 15-52. As is clear from the discussions with respect to claim 1, none of the text cited by the Examiner nor the corresponding figures in Webster describes a differential output except maybe transistors Q101, Q102. However, Webster does not teach first nodes of first **transistors** being coupled together and first nodes of second **transistors** being coupled together to form a differential output (emphasis added to show that the element "transistors" is plural).

Since Webster does not make up for the teaching deficiencies of Chen, the combination of Chen in view of Webster does not teach each and every element as set forth in claim 22. Accordingly, Applicants have successfully traversed the obviousness rejection with respect to claim 22 and its dependent claims (i.e., claims 23-38, 40 and 41).

It is respectfully requested that the rejection under 35 U.S.C. § 103(a) be withdrawn with respect to claims 22-28, 40 and 41.

Furthermore, although the Examiner alleges otherwise, Chen does not teach each and every element as set forth in claims 23-38, 40 and 41. For example, claim 26 recites that "the first nodes each comprises a drain". Since Chen does not teach first nodes as set forth in claim 22, Chen does not teach first nodes, each comprising a drain. Thus, Chen does not render obvious the subject matter recited in claim 26. In another example, claim 32 recites that "the bias circuit generates a bias current which is substantially independent of temperature". The Examiner maintains that col. 3, line 47 to col. 4, line 19 of Chen teaches these elements. However, the cited text does not even mention temperature and certainly does not teach a bias current which is substantially independent of temperature. Thus, Chen does not render obvious the subject matter recited in claim 32. In yet another example, claim 33 recites

that "the bias circuit comprises a first bias circuit having a first bias current exhibiting a positive temperature coefficient, a second bias circuit having a second bias current exhibiting a negative temperature coefficient, and a summer to sum the first and second bias currents, the summed first and second bias currents being applied to the switch control input". The Examiner maintains that col. 4, lines 3-67; col. 5, lines 3-45 and col. 7, lines 23-67 teach these elements. However, the cited text is silent as to, for example, a first bias current exhibiting a positive temperature coefficient and a second bias current exhibiting a negative temperature coefficient. Thus, Chen does not render obvious the subject matter as recited in claim 33. For at least these additional reasons, the obvious rejection cannot be maintained.

C. Claims 42-59, 61 and 62

To maintain an obvious rejection, each and every element must be taught by Chen in view of Webster as alleged by the Examiner. Applicants respectfully disagree that, as alleged by the Examiner, Chen in view of Webster teaches each and every element. For example, Chen in view of Webster as alleged by the Examiner does not teach each and every element as recited in claim 42.

The Examiner alleges that Chen teaches each and every element as set forth in claim 42 except "a current switch coupled to the current control input of one of the amplifying stages to selectively switch said one of the amplifying stages in or out of the circuit". To make up for the teaching deficiencies of Chen, the Examiner further alleges that Webster teaches at least these elements. To support this assertion, the Examiner cites the same text as before with respect to the rejection of claims 1 and 22, namely, Webster at col. 1, line 41 to col. 2, line 42; col. 6, line 62 to col. 7, line 66; and col. 12, lines 15-52. Applicants respectfully submit that the cited text and corresponding figures in Webster do not teach selectively switching an amplifying stage of a plurality of amplifying stages in or out of a circuit. Furthermore, Webster does not teach "a current switch coupled to the current control input of one of the amplifying stages to selectively switch said one of the amplifying stages in or out of the circuit".

Since Webster does not make up for the teaching deficiencies of Chen, the combination of Chen in view of Webster does not teach each and every element as set forth in claim 42. Accordingly, Applicants have successfully traversed the obviousness rejection with respect to claim 42 and its dependent claims (i.e., claims 43-59, 61 and 62).

It is respectfully requested that the rejection under 35 U.S.C. § 103(a) be withdrawn with respect to claims 42-59, 61 and 62.

Furthermore, although the Examiner alleges otherwise, Chen does not teach each and every element as set forth in claims 43-59, 61 and 62. Since claims 43-59, 61 and 62 recite many of the same or similar elements as recited in claims 23-38, 40 and 41 and since the Examiner used the same or similar arguments in rejecting claims 43-59, 61 and 62 as were used in rejecting claims 23-38, 40 and 41, Applicants respectfully make the same or similar arguments with respect to claims 43-59, 61 and 62 as were made with respect to claims 23-38, 40 and 41. For at least the above reasons, Chen does not render obvious the subject matter recited in claims 43-59, 61 and 62. For at least these additional reasons, the obvious rejection cannot be maintained.

D. Claims 63-79

Applicants respectfully draw the attention of the Examiner to page 14 of the Office Action in which ONLY Chen was cited in the rejection, which is presumably an obviousness rejection.

Chen does not teach each and every element as set forth in claim 63. For example, claim 63 recites "a digitally programmable power level and a matching circuit which is substantially independent of the programmed power level". The Examiner maintains that these elements are illustrated in FIGS. 3 and 4 and described in col. 2, lines 41-61; col. 3, lines 38-57; and col. 5, lines 3-32 of Chen. Applicants have carefully reviewed the cited portions of Chen and cannot find support for a digitally programmable power level and a matching circuit and, in particular, a matching circuit that is substantially independent of the programmed power level. For at least the above reasons, Chen does not render obvious the subject matter recited in claim 63 and its dependent claims (i.e., claims 64-79).

Furthermore, Chen does not teach each and every element as set forth in claims 64-79. Since claims 64-79 recite many of the same or similar elements as recited in claims 23-38, 40 and 41 and since the Examiner used the same or similar arguments in rejecting claims 64-79 as were used in rejecting claims 23-38, 40 and 41, Applicants respectfully make the same or similar arguments with respect to claims 64-79 as were made with respect to claims 23-38, 40 and 41. For at least the above reasons, Chen does not render obvious the subject matter recited in claims 64-79.

It is therefore respectfully requested that the rejection be withdrawn with respect to claims 63-79.

E. Claims 80-94

Applicants respectfully draw the attention of the Examiner to page 16 of the Office Action in which ONLY Chen was cited in the rejection, which is presumably an obviousness rejection.

Chen does not teach each and every element as set forth in claim 80. For example, claim 80 recites "switching means for switching one of the amplifying stages in or out of the amplifier to program power of the

amplifier". Chen describes an op amp with an input stage 28 and an output stage 34. The input stage includes a first differential pair MP1, MP2 and a complementary second differential pair MN1, MN2. See, e.g., FIG. 3; col. 3, lines 38-45; and col. 4, lines 3-10 of Chen. Thus, Chen describes two stages of an op amp. However, neither the input stage 28 nor the output stage 34 can be switched in or out of the circuit as set forth by claim 42. For example, a "switching/current sense" circuit 32 merely provides a bias current needed to make transistors MN1/MN2 active. See col. 3, lines 60-62 of Chen. However, the circuit 32 does not selectively switch the input stage 28 in or out of the circuit. In fact, the input stage 28 is always in the circuit whether or not the circuit 32 provides a bias current to transistors MN1/MN2. Since the input stage 28 is always active and cannot be switched in or out of the circuit, the output stage 34 receives a signal from the input stage 28, thereby causing the output stage 34 to also be active. Thus, the output stage 34 cannot be selectively switched in or out of the circuit. Thus, Chen does not teach at least these elements as set forth in claim 80. Furthermore, claim 80 recites "matching means for matching a load coupled to an output of the amplifier, the matching means being substantially independent of the programmed power". Since there is no mention of the load coupled to the output stage 34 of the op amp, Chen does not teach any type of matching with respect to such a load. Instead, Chen is merely concerned with trimming an op amp offset voltage. For at least the above reasons, Chen does not render obvious the subject matter recited in claim 80 and its dependent claims (i.e., claims 81-94).

Furthermore, Chen does not teach each and every element as set forth in claims 81-94. Since claims 81-94 recite many of the same or similar elements as recited in claims 23-38, 40 and 41 and since the Examiner used the same or similar arguments in rejecting claims 81-94 as were used in rejecting claims 23-38, 40 and 41, Applicants respectfully make the same or similar arguments with respect to claims 81-94 as were made with respect to claims 23-38, 40 and 41. For at least the above reasons, Chen does not render obvious the subject matter recited in claims 81-94.

It is therefore respectfully requested that the rejection be withdrawn with respect to claims 80-94.

II. REJECTION OF CLAIMS 19, 39, 60 and 95 UNDER 35 U.S.C. § 103(a)

Claims 19, 39, 60 and 95 stand rejected under 35 U.S.C. § 103(a) as being obvious over Chen in view of Webster and further in view of U.S. Patent No. 6,175,279 B1 ("Ciccarelli"). Applicants respectfully traverse the rejection.

Neither Chen, Webster nor Ciccarelli, alone or in combination, teaches or suggests each and every element as set forth in claims 19, 39 and 60. For example, claims 19, 39 and 60 recite that either the common differential output or the differential output "comprises first and second outputs, and the matching circuit comprises an inductor having a first end coupled to the first output and a capacitor having a first end coupled to the second output, the inductor and capacitor each having second end coupled together". The Examiner admits that Chen and Webster do not teach or suggest at least these elements of claims 19, 39 and 60. See Office Action at page 19. On the other hand, the Examiner maintains that Ciccarelli teaches or suggests these elements and offers FIG. 5A as well as supporting text in Ciccarelli as evidence in support of the rejection. Nevertheless, at least these elements are not taught or suggested by Ciccarelli. For example, Ciccarelli does not even teach or suggest a differential output or a common differential output in FIG. 5A and thus does not teach or suggest a first output and a second output. Instead, FIG. 5A shows a single-ended low-noise amplifier, thus teaching away from a differential output or a common differential output. FIG. 5A merely shows only one output, RF OUTPUT, to which only capacitor 1536 is coupled. Since Ciccarelli does not teach or suggest another output, Ciccarelli does not teach or suggest an inductor coupled to another output. For at least the above reasons, the Examiner has failed to demonstrate how the combination of Chen, Webster and Ciccarelli teaches or suggests each and every element as set forth in claims 19, 39 and 60.

Furthermore, neither Chen, Webster nor Ciccarelli, alone or in combination, teaches or suggests each and every element as set forth in claim 95. For example, claim 95 recites that "the amplifying stages comprises a differential output having first and second outputs, and the matching circuit comprises an inductor having a first end coupled to the first output and a capacitor having a first end coupled to the second output, the inductor and capacitor each having second end coupled to the amplifier output". The Examiner admits that Chen and Webster do not teach or suggest at least these elements of claim 95. See Office Action at page 19 ("Claim 95 contains similar limitations addressed in claim 19, 39, 60, and therefore is rejected under a similar rationale"). On the other hand, the Examiner maintains that Ciccarelli teaches or suggests these elements and offers FIG. 5A as well as supporting text in Ciccarelli as evidence in support of the rejection. Nevertheless, at least these elements are not taught or suggested by Ciccarelli. For example, Ciccarelli does not even teach or suggest a differential output in FIG. 5A and thus does not teach or suggest a first output and a second output. Instead, FIG. 5A shows a single-ended low-noise amplifier, thus teaching away from a differential output. FIG. 5A shows only one output, RF OUTPUT, to which only

capacitor 1536 is coupled. Since Ciccarelli does not teach or suggest another output, Ciccarelli does not teach or suggest an inductor coupled to another output. For at least the above reasons, the Examiner has failed to demonstrate how the combination of Chen and Ciccarelli teaches or suggests each and every element as set forth in claim 95.

It is therefore respectfully requested that the rejection under 35 U.S.C. § 103(a) be withdrawn with respect to claims 19, 39, 60 and 95.

III. CONCLUSION

In view of at least the foregoing, it is respectfully submitted that the pending claims 1-95 are in condition for allowance. Should anything remain in order to place the present application in condition for allowance, the Examiner is kindly invited to contact the undersigned at the below-listed telephone number.

Please charge any required fees not paid herewith or credit any overpayment to the Deposit Account of McAndrews, Held & Malloy, Ltd., Account No. 13-0017.

Dated: March 4, 2005

Respectfully submitted,

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